THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering

ELEC 401 – Analog CMOS Integrated Circuit Design
Take-Home Midterm Exam
Due: Monday, November 8th, 2021 at 11:59 pm

This is an open book take-home exam and calculators are allowed. Please attempt to answer all problems. A blank sheet will not receive any marks! Please do not consult and/or discuss the questions and/or your solutions with anyone. Your solutions/answers should be based on your individual effort! Please also note that each question has its own transistor parameters.

Good luck!

This exam consists of 6 – 6/6 (= 5) questions and including the cover page has 6+6(=12) pages. Please check that you have a complete copy.

#	MAX	GRADE
1	20	
2	20	
3	20	
4	20	
5	20	
TOTAL	100	

Shanks Cole
Surname First name

54950860
Student Number

READ THIS

IMPORTANT NOTE:

Candidates guilty of any of the following, or similar, dishonest practices shall be liable to disciplinary action:

Speaking or communicating with other candidates or non-candidates regarding the exam questions.

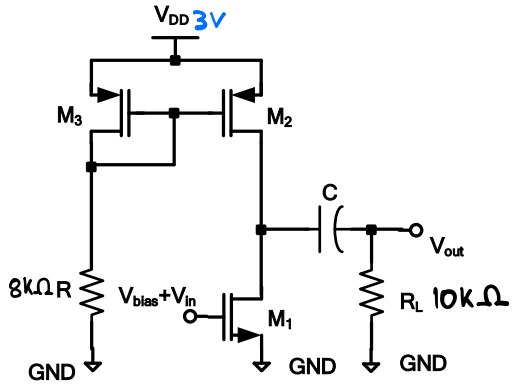
Purposely exposing their solution to the view of other candidates.

The plea of accident or forgetfulness shall not be received.

Q1 Incomplete
Q2 Incomplete
Q3 Incomplete
Q4 DONE
Q5 DONE

1. In the following amplifier, assume the decouple capacitor C is large enough so that it can be considered a short circuit for the small-signal analysis. Furthermore, assume that:

$\lambda_{(NMOS)}=0\ V^{-1}$, $\lambda_{(PMOS)}=0V^{-1}$, $V_{DD}=3.0$ V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5V$, $\mu_n C_{ox}=1mA/V^2$, $\mu_p C_{ox}=0.25\ mA/V^2$, $(W/L)_3=8$, and $(W/L)_2=32$, R=8 kΩ and R_L=10 kΩ. The DC component of the input signal is V_{bias} and the small-signal component of the input is V_{in}.



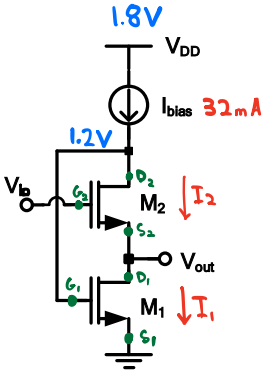
a) Assuming that the magnitude of the small-signal gain (magnitude of V_{out}/V_{in}) is 40 V/V find V_{bias} and $(W/L)_1$ **[14 marks]**
b) For this circuit, for transistors M_1 and M_2 to operate in saturation, find the minimum and maximum voltage level at the drain of M_1. **[6 marks]**.

V_{bias}= _____V, $(W/L)_1$=_____, $V_{DS1,min}$= _____V, $V_{DS1,max}$= _____V

2. In the follwing circuit assume that:
$\lambda_{(NMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 1.8V$, $I_{bias} = 32mA$, $V_{TH(NMOS)} = 0.4V$, and $\mu_n C_{ox} = 1\ mA/V^2$.
Furthermore, assume that both transistors are supposed to operate in saturation region and their sizes are: $(\frac{W}{L})_1 = 100$ and $(\frac{W}{L})_2 = 400$.

a) Find the minimum and maximum dc voltage levels at node V_{out}. **[8 marks]**
b) Find the allowable minimum and maximum dc voltage level of the input node. **[8 marks]**
c) If γ was not zero, would the allowable input signal swing range change, and if so, why? **[4 marks]**

$V_b = V_{in}$



$-V_{DS} > V_{GS} - V_{th}$ SATURATION (Active)

channel is pinched off.

$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$

$V_D - V_S > V_G - V_S - V_{th}$

$V_{GD} \leq V_{th}$

$V_b - 1.2V \leq 0.4$

$V_b \leq 1.6V$

Saturation:

M_2: $V_b - V_{GS_1} \leq V_{thn} \rightarrow V_b \leq V_{GS_1} + V_{thn}$

M_1: $V_{GS_1} - V_o \leq V_{th} \rightarrow V_{GS_1} - (V_b - V_{GS_2}) \leq V_{thn}$

$V_{GS_1} + V_{GS_2} - V_{thn} \leq V_b$

Requirement on V_b:

$V_{GS_1} + V_{GS_2} - V_{thn} \leq V_b \leq V_{GS_1} + V_{thn}$

$\therefore V_{GS_1} + V_{GS_2} - V_{thn} \leq V_{GS_1} + V_{thn}$

$V_{GS_2} - V_{thn} \leq V_{thn}$

$V_{eff_2} \leq V_{thn} \rightarrow \boxed{V_b - V_o \leq 0.8V}$

Currents:

M_2: $32mA = \frac{1}{2} \cdot 1\times10^{-3} \cdot 400 \cdot (V_{GS_2} - 0.4)^2 \rightarrow V_{GS_2} = 0.8V \rightarrow V_{eff_2} = 0.4V$

M_1: $32mA = \frac{1}{2} \cdot 1\times10^{-3} \cdot 100 \cdot (V_{GS_1} - 0.4)^2 \rightarrow V_{GS_1} = 1.2V \rightarrow V_{eff_1} = 0.8V$

$\hookrightarrow V_{G_1} = V_{D_2} = 1.2V$

Requirements for Saturation:

M_2: $V_b - 1.2V \leq 0.4V$

$\hookrightarrow \boxed{V_b \leq 1.6V}$ (1)

(b) if $V_b = 1.6V \rightarrow V_o = V_b - 0.8V = 0.8V$ ∴ V_o can also only be 0.8V to satisfy Saturation Requirements of M_2, M_1

$V_o(Max) = 0.8V$
$V_o(Min) = 0.8V$

(c)

M_1: $1.2V - V_o \leq 0.4V$

$V_b - V_o = 0.8V$

$\therefore V_o = V_b - 0.8V$

$1.2V - V_b + 0.8V \leq 0.4V$

$V_b \geq 1.2V + 0.8V - 0.4V$

$\boxed{V_b \geq 1.6V}$ (2)

$V_{in}(Max) = 1.6V$
$V_{in}(Min) = 1.6V$

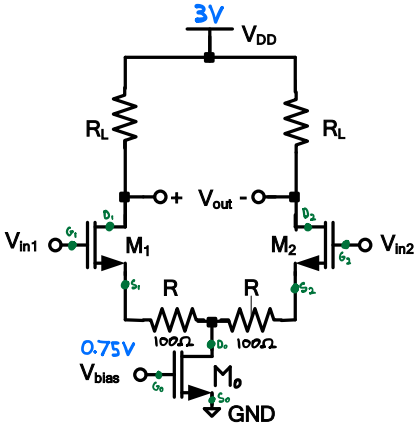
- Bounded on both sides by 1.6V → No voltage swing
$V_b = 1.6V$

$V_{out,min}$= _____V, $V_{out,max}$ =_____, $V_{in,min}$= _____V, $V_{in,max}$= _____V

For $\gamma \neq 0$ would allowable input signal swing range change and why?

3. Consider the following differential amplifier.

Saturation Equations:



Assume all transistors are operating in saturation region and $\lambda=\gamma=0$, $V_{DD}=3$ V, $V_{TH(NMOS)}=0.5$ V, $\mu_n C_{ox}=1$ mA/V^2, R=100 Ω, $(W/L)_1=(W/L)_2=16$ and $(W/L)_0=32$. Also, assume that the $V_{bias}=0.75$ V and the circuit is symmetric.

a) What should the value of R_L be if the magnitude of the differential voltage gain of the circuit is 4 V/V **[10 marks]**

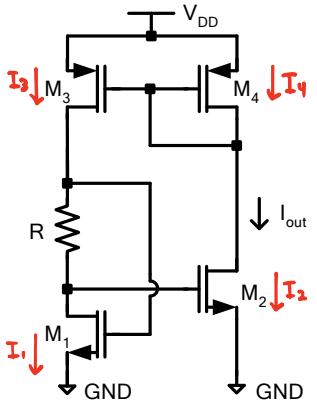
b) For the circuit to operate properly (i.e., all transistors operate in their saturation region), what are the minimum and maximum values of the input common-mode voltage (i.e., input DC voltage) **[10 marks]**

R_L:_____, $V_{in,cm\ (min)}$: _____, $V_{in,cm\ (max)}$: _____

4. In the following circuit, assuming that all transistors are in saturation, $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$, and $\lambda = \gamma = 0$:

$I_3 = I_{out} = I_1$

i) Find an expression for I_{out} in terms of R, transistor parameters (e.g., μ and C_{ox}), and transistor sizes **[10 marks].**
ii) What would be the percentage change in I_{out} if V_{DD} is increased by 10%. **[5 marks]**
iii) How would the expression for I_{out} derived in part (i) change if $\gamma \neq 0$ and why? **[5 marks]**



(i) $I_o = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{thn})^2$

$V_{GS2} = V_{thn} + \sqrt{\frac{2I_o}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} \rightarrow V_{GS1} = V_{thn} + \sqrt{\frac{2I_o}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}}$

$V_{GS1} - V_{GS2} = R \cdot I_o$

$\left(V_{thn} + \sqrt{\frac{2I_o}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}}\right) - \left(V_{thn} + \sqrt{\frac{2I_o}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}}\right) = R \cdot I_o$

$\sqrt{\frac{2I_o}{\mu_n C_{ox}}} \cdot \left(\sqrt{\frac{1}{\left(\frac{W}{L}\right)_1}} - \sqrt{\frac{1}{\left(\frac{W}{L}\right)_2}}\right) = R I_o$

$\frac{2I_o}{\mu_n C_{ox}} \cdot \left(\sqrt{\frac{1}{\left(\frac{W}{L}\right)_1}} - \sqrt{\frac{1}{\left(\frac{W}{L}\right)_2}}\right)^2 = R^2 \cdot I_o^2$

$\rightarrow I_o = \frac{2}{R^2 \mu_n C_{ox}} \cdot \left(\sqrt{\frac{1}{\left(\frac{W}{L}\right)_1}} - \sqrt{\frac{1}{\left(\frac{W}{L}\right)_2}}\right)^2$

(ii) NONE, I_o is independent of V_{DD}

(iii) No Change, no body effect $V_{SB_1} = 0$ $V_{SB_2} = 0$

5. The 5-transistor operational transconductance amplifier (that is, the differential to single-ended structure with active current mirror load that we discussed in class) is a popular choice in designing operational amplifiers. Consider the following two-stage amplifier based on the topology shown below (first stage is a differential to signle-ended amplifier followed by the second stage which is a common-source amplifier) with the following design specifications:

- V_{DD}=3 V
- Total power consumption of 3 mW
- Output swing of 2.6 V
- Magnitude of the overall gain: 1000 V/V
- L = 0.4µm for all the device

Use the following assumptions for the design:

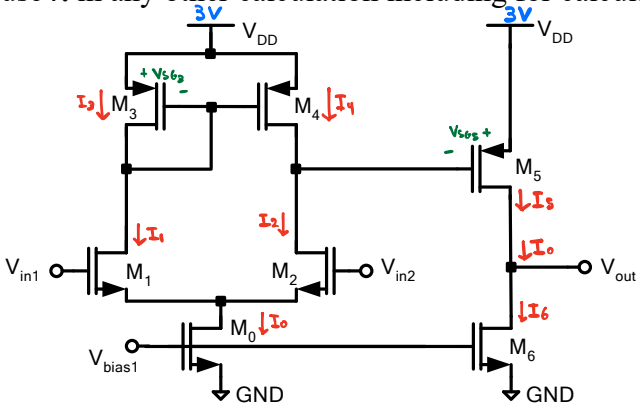
- Allocate equal effective voltages for M_5 and M_6 $V_{oD5} = V_{oD6}$
- Assume the bias current of M_0 and M_6 are equal.
- For the purpose of DC analysis, assume V_{SG3}=V_{SG5}

The technology parameters are:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0.1\ V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5$ V, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox} = 0.5\ mA/V^2$.

Note: Use the parameter λ only for calculating the r_o of the transistors and for the small-signal gain. **<u>Do not</u>** use λ in any other calculation including for calculating bias currents.

$P = IV$

$\therefore 3mW = I_o \cdot$



Find V_{bias1}, and all the transistor widths (i.e., W_0, W_1, W_2, W_3, W_4, W_5, W_6). **[20 marks]**

<u>Output Swing:</u>

$V_{DD} - |V_{oD5}| - V_{oD6} \rightarrow 2.6V = 3 - 2\cdot|V_{oD5}| \rightarrow |V_{oD5}| = V_{oD6} = 0.2V$, $V_{SG3} = V_{SG5} \rightarrow |V_{oD3}| = 0.2V$

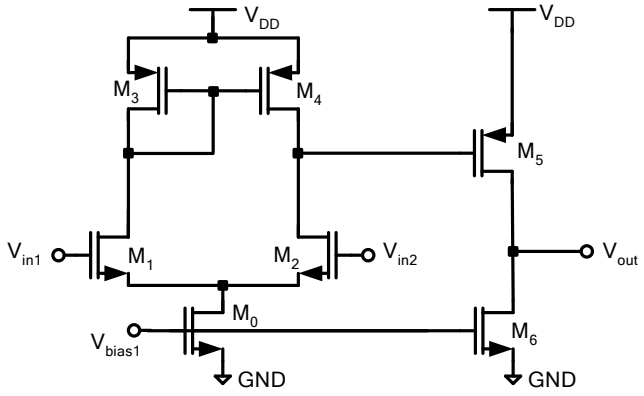
$I_{out} = I_5 = \frac{1}{2}\cdot\frac{3mW}{3V} = 0.5mA \rightarrow 0.5mA = \frac{1}{2}\cdot 0.5\times10^{-3}\cdot\left(\frac{W}{0.4um}\right)_5\cdot 0.2^2 \rightarrow$ **$W_5 = 20um$**

<u>I_6</u>: $0.5mA = \frac{1}{2}\cdot 1\times10^{-3}\cdot\left(\frac{W}{0.4um}\right)_6\cdot 0.2^2 \rightarrow$ **$W_6 = 10um$**

<u>I_3</u>: $\frac{1}{2}\cdot 0.5mA = \frac{1}{2}\cdot 0.5\times10^{-3}\cdot\left(\frac{W}{0.4um}\right)_3\cdot 0.2^2 \rightarrow$ **$W_3 = 10um$** → **$W_4 = 10um$** (M_4 is the same)

<u>I_o</u>: $0.5mA = \frac{1}{2}\cdot 1\times10^{-3}\cdot\left(\frac{W}{0.4um}\right)_o\cdot 0.2^2 \rightarrow$ **$W_o = 10um$**

For your convenience the circuit diagram and transistor parameters are replicated here:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0.1\ V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5$ V, $\mu_n C_{ox} = 1$ mA/V^2, $\mu_p C_{ox} = 0.5$ mA/V^2.



$r_{o2} = \frac{1}{0.1 \cdot 0.25mA} = 40k\Omega$, $r_{o4} = \frac{1}{0.1 \cdot 0.25mA} = 40k\Omega$

$r_{o6} = \frac{1}{0.1 \cdot 0.5mA} = 20k\Omega$, $r_{o5} = \frac{1}{0.1 \cdot 0.5mA} = 20k\Omega$

Overall Gain:

$|A_v| = g_{m1}(r_{o2} \| r_{o4}) \cdot g_{m5}(r_{o5} \| r_{o6}) \rightarrow 1000 = g_{m1} \cdot (40k\Omega \| 40k\Omega) \cdot \frac{2 \cdot 0.5 \times 10^{-3}}{0.2} \cdot (20k\Omega \| 20k\Omega)$

$\rightarrow g_{m1} = 1 \times 10^{-3} \rightarrow 1 = \sqrt{2 \cdot 1 \cdot \left(\frac{W}{0.4um}\right)_1 \cdot I_{D1}} \rightarrow$ **$W_1 = 0.8um$**

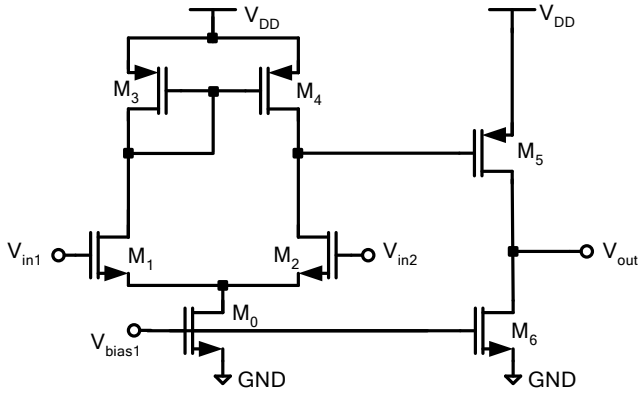
M_2 is the same $\rightarrow$ **$W_2 = 0.8um$**

M_0: $V_{eff_0} = (V_{bias1} - V_{thn})$

$0.2 = V_{bias1} - 0.5$

$\therefore$ **$V_{bias1} = 0.7V$**

For your convenience the circuit diagram and transistor parameters are replicated here:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0.1\ V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5$ V, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox} = 0.5\ mA/V^2$.



V_{bias1}= 0.7 V, W_0= 10 µm, W_1= 0.8 µm, W_2= 0.8 µm

W_3= 10 µm, W_4= 10 µm, W_5= 20 µm, W_6= 10 µm